CUSTOMER NO. 32914

PATENT APPLICATION
Docket No. 361170-1028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of: Busson, et al.	Confirmation No.: 5448
Serial No.: 10/814,621	Group No.: 2426
Filed: March 31, 2004	Examiner: F. Peng

For: ELECTRONIC COMPONENT ALLOWING THE DECODING OF DIGITAL TERRESTRIAL OR CABLE TELEVISION SIGNALS

MAIL STOP Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the final Office Action dated September 29, 2010 and the Advisory Action dated December 2, 2010, the due date for response being January 29, 2011 (with a one month extension of time hereby requested), please consider the following claims and Remarks:

LISTING OF CLAIMS

Claims 1-51. (Canceled).

52. (Currently Amended) The apparatus of claim 60 ~~51~~ wherein the digital baseband decimating filter is a Nyquist digital filter having a cutoff frequency equal to the frequency half-width of one channel.

52. (Second Occurrence) (Canceled).

53. (Currently Amended) The apparatus of claim 60 ~~51~~, wherein the device is a receiver of digital terrestrial or cable television signals.

54. (Currently Amended) The apparatus of claim 60 ~~53~~, wherein the analog signal is one of a digital terrestrial or cable television signal.

55. (Currently Amended) The apparatus of claim 60 ~~51~~, wherein the first and second ports carry signals on and off, respectively, the integrated circuit substrate.

56. (Currently Amended) The apparatus of claim 60 ~~51~~ wherein the channels of the analog signal extend over a frequency span and wherein the upconversion device upconverts the received analog signal to a frequency that is higher than an upper limit of the frequency span.

57. (Previously Presented) The apparatus of claim 56 wherein the upconversion device upconverts the received analog signal to a frequency that is the sum of a desired channel frequency plus the upper limit of the frequency span.

58. (Currently Amended) The apparatus of claim 60 ~~51~~ wherein the surface acoustic wave filter is a bandpass filter having a pass band of at least two times a frequency width of one channel.

59. (Currently Amended) The apparatus of claim 60 ~~51~~ wherein the integrated circuit substrate additionally includes the following circuit component: means for delivering a stream of data packets corresponding to information in a desired channel of the analog signal from the filtered digital baseband signal.

60. (Currently Amended) Apparatus ~~The apparatus of claim 51~~, comprising:

a surface acoustic wave filter; and

an integrated circuit embodied on a single monolithic substrate in which each of the following circuit components are fabricated on that single monolithic substrate:

an input adapted to receive an analog signal including a plurality of channels;

an upconversion device to upconvert the received analog signal;

a first port for off substrate connection to an input of the surface acoustic wave filter and coupled to receive the upconverted analog signal for application to the surface acoustic wave filter;

a second port for off substrate connection to an output of the surface acoustic wave filter to receive a filtered upconverted signal from the surface acoustic wave filter; and

a downconversion device coupled to the second port to downconvert the filtered upconverted signal to a baseband signal centered at zero frequency;

a baseband filtering circuit that filters the baseband signal to generate a filtered analog baseband signal, the baseband filtering circuit having an upper cutoff frequency greater than a frequency half-width of one channel;

an analog-to-digital converter circuit that converts the filtered analog baseband signal to a digital baseband signal, the analog-to-digital converter circuit having a sampling frequency which is at least ten times the upper cutoff frequency of the baseband filtering circuit; and

a digital baseband decimating filter that filters the digital baseband signal to generate a filtered digital baseband signal;

wherein the single monolithic substrate further includes an oxide layer on a rear surface of the substrate, the apparatus further comprising: a metal plate glued to the oxide layer on the rear surface of the substrate to form a first plate of a capacitor, wherein a second plate of the capacitor is formed by the single monolithic substrate.

61. (Previously Presented) The apparatus of claim 60 wherein the metal plate is a grounded metal plate and the capacitor functions to absorb high-frequency current spikes.

62. (Currently Amended) Apparatus ~~The apparatus of claim 51~~, comprising:

a surface acoustic wave filter; and

an integrated circuit embodied on a single monolithic substrate in which each of the following circuit components are fabricated on that single monolithic substrate:

an input adapted to receive an analog signal including a plurality of channels;

an upconversion device to upconvert the received analog signal;

a first port for off substrate connection to an input of the surface acoustic wave filter and coupled to receive the upconverted analog signal for application to the surface acoustic wave filter;

a second port for off substrate connection to an output of the surface acoustic wave filter to receive a filtered upconverted signal from the surface acoustic wave filter; and

a downconversion device coupled to the second port to downconvert the filtered upconverted signal to a baseband signal centered at zero frequency;

a baseband filtering circuit that filters the baseband signal to generate a filtered analog baseband signal, the baseband filtering circuit having an upper cutoff frequency greater than a frequency half-width of one channel;

an analog-to-digital converter circuit that converts the filtered analog baseband signal to a digital baseband signal, the analog-to-digital converter circuit having a sampling

frequency which is at least ten times the upper cutoff frequency of the baseband filtering circuit; and

a digital baseband decimating filter that filters the digital baseband signal to generate a filtered digital baseband signal;

wherein the single monolithic substrate has a first type of conductivity, and wherein elements performing digital processing are disposed in a part of the substrate that is isolated from the remaining part of the substrate by a semiconducting barrier having a second type of conductivity different from the first type of conductivity, and wherein the semiconducting barrier is adapted to be biased by a bias voltage different from that supplying the isolated part of the substrate.

63. (Previously Presented) A circuit, comprising:

an input adapted to receive an analog signal including a plurality of channels;

an upconversion device adapted to upconvert the received analog signal;

a bandpass filter adapted to filter the received analog signal and generate a filtered upconverted signal comprising information from at least one channel, wherein the bandpass filter is a surface acoustic wave filter;

a downconversion device adapted to downconvert the filtered upconverted signal to an analog baseband signal centered at zero frequency;

an analog low pass filter adapted to filter the analog baseband signal and generate a filtered analog baseband signal, the analog low pass filter having an upper cutoff frequency greater than a frequency half-width of one channel;

an analog-to-digital converter adapted to convert the analog baseband signal to a digital baseband signal, the analog-to-digital converter having a sampling frequency which is at least ten times the upper cutoff frequency of the second filter; and

a digital decimating low pass filter adapted to filter the digital baseband signal and generate a filtered digital baseband signal, the digital decimating low pass filter having a cutoff frequency substantially equal to the frequency half-width of one channel;

wherein all of the recited components of the circuit, with the exception of the surface acoustic wave filter, are implemented on a single integrated circuit chip and the surface acoustic wave filter is connected to the single integrated circuit chip as an off-chip component;

wherein the single integrated circuit chip further includes an oxide layer on a rear surface of a substrate of the chip, the apparatus further comprising: a metal plate glued to the oxide layer on the rear surface of the substrate to form a first plate of a capacitor, wherein a second plate of the capacitor is formed by the substrate.

Claims 64-66. (Canceled).

67. (Previously Presented) The circuit of claim 63 wherein the metal plate is a grounded metal plate and the capacitor functions to absorb high-frequency current spikes.

68. (Previously Presented) A circuit, comprising:

an input adapted to receive an analog signal including a plurality of channels;

an upconversion device adapted to upconvert the received analog signal;

a bandpass filter adapted to filter the received analog signal and generate a filtered upconverted signal comprising information from at least one channel, wherein the bandpass filter is a surface acoustic wave filter;

a downconversion device adapted to downconvert the filtered upconverted signal to an analog baseband signal centered at zero frequency;

an analog low pass filter adapted to filter the analog baseband signal and generate a filtered analog baseband signal, the analog low pass filter having an upper cutoff frequency greater than a frequency half-width of one channel;

an analog-to-digital converter for converting the analog baseband signal to a digital baseband signal, the analog-to-digital converter having a sampling frequency which is at least ten times the upper cutoff frequency of the second filter; and

a digital decimating low pass filter adapted to filter the digital baseband signal and generate a filtered digital baseband signal, the digital decimating low pass filter having a cutoff frequency substantially equal to the frequency half-width of one channel;

wherein all of the recited components of the circuit, with the exception of the surface acoustic wave filter, are implemented on a single integrated circuit chip and the surface acoustic wave filter is connected to the single integrated circuit chip as an off-chip component;

wherein the single integrated circuit chip is formed of a substrate having a first type of conductivity, and wherein elements performing digital processing are disposed in a part of the substrate that is isolated from the remaining part of the substrate by a semiconducting barrier having a second type of conductivity different from the first type of conductivity, and wherein

the semiconducting barrier is adapted to be biased by a bias voltage different from that supplying the isolated part of the substrate.

69. (Previously Presented) The circuit of claim 63, further including means for decoding the filtered digital baseband signal to deliver a stream of data packets corresponding to information in a selected one of the channels.

70. (Previously Presented) The circuit of claim 63, wherein the upconversion device and downconversion device in combination comprises a zero intermediate frequency dual conversion tuner.

Claims 71 -72. (Canceled).

73. (Previously Presented) An electronic component, comprising:

a tuning module of the zero intermediate frequency dual conversion, upconversion stage then downconversion stage, type having:

an input adapted to receive digital terrestrial or cable television analog signals composed of several channels,

a bandpass filter of the surface acoustic wave type disposed between the upconversion and downconversion stages and adapted to output a filtered analog signal containing information of a desired channel and adjacent channel information, and

a baseband filtering stage disposed on two quadrature output paths of the downconversion stage adapted to perform a low pass filtering of the adjacent channel information, the baseband filtering stage having an upper cutoff frequency greater than a frequency half-width of the desired channel;

a multibit analog/digital conversion stage coupled to an output of the baseband filtering stage, the multibit analog/digital conversion stage having a sampling frequency which is at least ten times the upper cutoff frequency of the baseband filtering stage; and

a digital processing block comprising:

a stage adapted to correct the defects of phase- and amplitude-pairing of the two quadrature output paths, and

a channel decoding digital module, linked to the output of the stage adapted to correct defects, and comprising:

a demodulation stage,

a digital decimation filtering stage having a cutoff frequency substantially equal to the frequency half-width of the desired channel adapted to eliminate the adjacent channel information, and

an error correcting stage adapted to deliver a stream of data packets corresponding to the information conveyed by the desired channel.

74. (Previously Presented) The component according to Claim 73, wherein, with the exception of the surface acoustic wave filter of the tuning module, all circuits within the tuning

module, the analog/digital conversion stage and the digital processing block are disposed within an integrated circuit that is fabricated on a single monolithic substrate.

75. (Previously Presented) The component according to Claim 74, wherein the single integrated circuit chip further includes an oxide layer on a rear surface of a substrate of the chip, the apparatus further comprising:

a metal plate glued to the oxide layer on the rear surface of the substrate to form a first plate of a capacitor, wherein a second plate of the capacitor is formed by the substrate.

76. (Previously Presented) The component according to Claim 75, wherein the metal plate is a grounded metal plate and the capacitor functions to absorb high-frequency current spikes.

77. (Previously Presented) The component according to Claim 74, wherein the single integrated circuit chip is formed of a substrate having a first type of conductivity, and wherein elements performing digital processing are disposed in a part of the substrate that is isolated from the remaining part of the substrate by a semiconducting barrier having a second type of conductivity different from the first type of conductivity, and wherein the semiconducting barrier is adapted to be biased by a bias voltage different from that supplying the isolated part of the substrate.

78. (Previously Presented) The component according to Claim 73, wherein the first frequency transposition stage is able to receive a first transposition signal having a frequency equal either to the sum of the frequency of the desired channel and of a first transposition frequency greater than the upper limit of the said frequency span, or the difference between the said first transposition frequency and the frequency of the desired channel, and wherein the second frequency transposition stage is able to receive a second transposition signal having the said first transposition frequency, in that the passband of the surface acoustic wave filter is of the order of two to three times the frequency width of a channel, and wherein the bandpass filtering stage possesses an upper cutoff frequency around 20% greater than the frequency half-width of a channel.

79. (Previously Presented) The component according to Claim 78, wherein the passband of the surface acoustic wave filter is of the order of 20 MHz.

80. (Previously Presented) The component according to Claim 73, wherein the resolution of the multibit analog/digital conversion stage is greater than or equal to 4 bits.

REMARKS

Claims 63, 67-70 and 73-80 have been allowed.

Claims 60-62 are objected to dependent claims. Claims 60 and 62 have been amended into independent form to include the limitations of base claim 51. Claims 60-62 are now in condition for allowance.

Claims 51, 53-59, 63-65 and 69-72 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Uramoto, Keate, Birleson and MPEP 2144.04. Claim 52 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Uramoto, Keate, Birleson, MPEP 2144.04 and Misaizu.

Claim 51 has been canceled.

Claims 52-59 have been amended to depend from allowable claim 60.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

The Office is authorized to charge any additional claim fees necessary for entry of this response to deposit account 07-0153 (reference 361170-1028).

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Respectfully submitted,

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